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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,156	08/20/2003	Shi-Dong Zhou	X-1477 US	5800

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,156	ZHOU ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *3-22,25-27,29 and 30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *3-22,25-27,29 and 30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kato et al. (U.S. Patent No. 6,492,850) in view of Zhou et al. (U.S. Patent No. 6,683,481).

In reference to claim 3, Kato discloses in Figure a power-on reset circuit (2) to generate a reset signal, comprising: a pull-up resistor connected between a supply voltage (VEXT) and a tracking node; a pull-down transistor connected between the tracking node and ground potential, the tracking node generating a voltage (POR) indicative of the reset signal; and a voltage divider circuit connected between the supply voltage (VEXT) and ground potential, the voltage divider circuit having a first ratioed voltage node coupled to the gate of the pull-down transistor. Kato does not disclose that the voltage divider comprises a third resistor and a shunt transistor. Zhou discloses in Figure 5 a power on reset circuit including a voltage divider having a first resistor (RE1) connected between the voltage supply (VDD) and the first ratioed voltage node (DD); and a second resistor (RE2) connected between the first ratioed voltage node (DD) and a second ratioed voltage node (EE); and a shunt transistor (503) connected between the second ratioed voltage node (EE) and ground potential, and having a gate responsive to the reset signal. It would have been obvious to one skilled in the art at

the time of the invention that the voltage divider circuit of Kato could be replaced with the voltage divider of Zhou for the advantage of preventing glitches from reaching the output signal (see Zhou column 3, line 67 through column 4, line 4). The same applies to claims 14, 25, 26-27, and 30 (wherein the voltage divider is seen to be the same as the means for generating the control voltage).

In reference to claim 4, this limitation is seen to be inherent in the operation of a POR circuit. The same applies to claim 15.

In reference to claim 5, Kato discloses that the power-up reset level comprises a first factor multiplied by a threshold voltage of the pull-down transistor, the first factor determined by the relative resistances of the first and second resistors. The same applies to claims 16 and 29.

In reference to claim 6, Zhou discloses that the power-up reset level comprises a second factor multiplied by a threshold voltage of the pull-down transistor (of Kato), the second factor determined by the relative resistances of the first and second and third resistors. The same applies to claim 17.

In reference to claim 7, Zhou discloses in Figure 5 that the first and second factors comprise ratios characterized by the voltage divider circuit (RE1, RE2, RE3, 503).

In reference to claim 8, Zhou discloses in Figure 5 that the shunt transistor (503) selectively shunts the third resistor (RE3) in response to the reset signal to provide hysteresis between the power-up reset level and the power-down reset level. The same applies to claim 18.

In reference to claim 9, Zhou discloses in Figure 5 wherein the power0up reset level and the power-down reset level is determined by the third resistor (RE3).

In reference to claim 10, Kato and Zhou disclose that the pull-down and shunt transistors comprise NMOS transistors. The same applies to claim 19.

In reference to claim 11, Kato discloses in Figure 1 a buffer circuit (the two inverters receiving signal POR) having an input coupled to the tracking node and an output to generate the reset signal. The same applies to claim 20.

In reference to claim 12, Kato discloses in Figure 1 that the buffer circuit comprises a first inverter having an input coupled to the tracking node, and having an output and a second inverter having an input coupled to the output of the first inverter and having an output to generate the reset signal. The same applies to claim 21.

In reference to claim 13, Zhou discloses in Figure 5 that the circuit is part of a programmable logic device. It is considered obvious to one of ordinary skill in the art that the circuit of Kato could also be implemented as part of a programmable logic device. The same applies to claim 22.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 7:00 AM to 4:30 PM and on alternate Fridays from 7:30 AM to 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC

June 10, 2005

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800